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PATENT APPLICATION  
TRANSMITTAL**

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First Inventor or Application Identifier

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Title

DUAL DAMASCENE STRUCTURE AND METHOD OF MAKING

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**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents

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1. ☒ Fee Transmittal Form (e.g. PTO/SB/17)  
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2. ☒ Specification Total Pages **17**

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a. ☒ Newly executed (original or copy)

b. ☐ Copy from a prior application (37 C.F.R. §1.63(d))  
(for continuation/divisional with box 15 completed)

i. ☐ DELETION OF INVENTOR(S)  
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in the prior application, see 37 C.F.R. §1.63(d)(2) and  
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The entire disclosure of the prior application, from which a copy of  
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part of the disclosure of the accompanying application and is hereby  
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**ACCOMPANYING APPLICATION PARTS**

6. ☒ Assignment Papers (cover sheet & document(s))  
7. ☐ 37 C.F.R. §3.73(b) Statement ☐ Power of Attorney  
(when there is an assignee)  
8. ☐ English Translation Document (if applicable)  
9. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations  
10. ☐ Preliminary Amendment  
11. ☐ White Advance Serial No. Postcard  
12. ☐ Small Entity Statement(s) ☐ Statement filed in prior application. Status still proper and desired.  
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☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no.:

Prior application information: Examiner: Group Art Unit:

16. Amend the specification by inserting before the first line the sentence:

☐ This application is a ☐ Continuation ☐ Division ☐ Continuation-in-part (CIP)  
of application Serial No. Filed on

☐ This application claims priority of provisional application Serial No. Filed

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195425US

TITLE OF THE INVENTION

DUAL DAMASCENE STRUCTURE AND METHOD OF MAKING

BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates to electrical connections in integrated semiconductor circuits. In particular, this invention relates to a dual damascene interconnect structure and to methods of making the interconnect structure.

Discussion of the Background

To form integrated circuits, discrete semiconductor devices must be wired together electrically. The electrical wiring used frequently includes damascene structures. Damascene structures are produced by forming grooves in an insulating layer and then filling the grooves with metal. Advances in damascene processing have led to processes characterized as dual damascene.

Dual damascene is a multi-level interconnection process in which, in addition to forming the grooves of single damascene, via openings (i.e., contact holes) are also formed. In one dual damascene process, an insulating layer is coated with a photoresist, which is exposed through a first mask with image pattern of the via openings. The pattern is anisotropically etched in the upper half of the insulating layer. The photoresist is then exposed through a second mask with an image pattern of conductive line openings, after being aligned with the first mask pattern to encompass the via openings. In anisotropically etching the openings for the conductive lines in the upper half of the insulating material, the via openings already present in the upper half are simultaneously etched and replicated in the lower half of the insulating material. After the etching is complete, both the vias and line openings are filled with metal. Dual damascene is an improvement over single damascene because it permits the filling of both the conductive grooves and vias with metal at the same time, thereby eliminating process steps.

A number of dual damascene processes have been developed, including processes using an insulating layer that includes an etch stop layer. In an example of such a process, a first layer of insulator is deposited over a first level of patterned metal to which electrical contacts are to be selectively established. The first layer is planarized, if the underlying structure is not formed using a damascene process, and then covered by an etch stop material. Contact holes are defined in the etch stop material by a first lithography at locations where vias are required. The first insulator layer is not etched at this time. A second insulator layer, having a thickness equal to the thickness of the second level of patterned metal of the multi-level structure being formed, is deposited over the etch stop material. The second insulator layer, in turn, is etched by a second photolithography down to the etch stop material to define desired wiring channels, some of which will be in alignment with the previously formed via holes in the etch stop material. In those locations where the via holes are exposed, the etching is continued into the first insulator layer to uncover the underlying first level of patterned metal. The horizontal channels and vertical holes etched into the second and first insulator layers are next overfilled with metal. As a final step, excess metal on top of the second insulator layer but not in the channels or holes is removed by etching or chemical-mechanical polishing.

In another example of a dual damascene process using an etch stop layer, a first layer of insulator is deposited over a first level of patterned metal to which electrical contacts are to be selectively formed. The first layer is planarized, if the prior structure is not formed using a damascene process, and then covered by an etch stop material. A second insulator layer, having a thickness equal to the thickness of the second level of patterned metal of the multi-level structure being formed, is deposited over the etch stop material. Contact holes are then defined on top of the second insulator layer by a first lithography at locations where vias are to be formed. The second insulator layer, the etch stop layer and the first insulator layer are etched at this time to form the via holes. A second photolithography is performed on the second insulator material to define desired wiring channels, some of which will be in alignment with the previously formed via holes. A second plasma etch process, requiring an etch selectivity between the second insulator material and the etch stop material, is used to form horizontal channels in the second insulator layer. The horizontal channels and the

vertical via holes are next overfilled with metal. As a final step, excess metal on top of the second insulator layer but not in the channels or holes is removed by etching or chemical-mechanical polishing.

In still another example of a dual damascene process using an etch stop layer, a first layer of insulator is deposited over a first level of patterned metal to which electrical contacts are to be selectively formed. The first layer is planarized, if the underlying structure is not formed using a damascene process, and then covered by an etch stop material. A second insulator layer, having a thickness equal to the thickness of the second level of patterned metal of the multi-level structure being formed, is deposited over the etch stop material. Horizontal channels are then defined on top of the second insulator layer by a first lithography at locations where metal conducting trenches are required. The second insulator layer is etched at this time, either selectively stopping at the etch stop layer or being timely controlled to reach the required trench depth. A second photolithography is performed on the second insulator material to define via openings, some of which will be in alignment with the previously formed channels. A second plasma etch process is performed to open the via holes. The horizontal channels in the second insulator layer and the vertical via holes are next overfilled with metal. As a final step, excess metal on top of the second insulator layer but not in the channels or holes is removed by etching or chemical-mechanical polishing. In conventional dual damascene processes, the etch stop layer used is typically silicon nitride.

Huang et al. U.S. 5,635,423 reports a modified dual damascene process in which an initial opening in a trench dielectric is enlarged while simultaneously extending a via opening through an etch stop layer and a via dielectric.

Avanzino et al. U.S. 5,795,823 reports the fabrication of conductive lines and connecting vias using dual damascene with only one mask pattern. This is also reported by Avanzino et al. in U.S. 5,614,765.

Yen U.S. 5,861,676, reports a method of forming interconnects and contacts between elements in a semiconductor or integrated circuit.

Dai et al U.S. 5,877,075 reports forming dual damascene patterns using a single photoresist process.

Dai U.S. 5,877,076 reports a dual damascene process using opposite type two-layered

photoresist.

Dai U.S. 5,882,996 discloses a method for patterning dual damascene interconnections using a developer soluble ARC interstitial layer.

In spite of known techniques for forming contacts and interconnects, increases in device density and demands for increased processing efficiency have spurred new efforts to effectively produce semiconductor interconnections.

### SUMMARY OF THE INVENTION

The present invention provides a dual damascene structure in which a conventional etch stop layer (e.g., of silicon nitride) is replaced with an etch stop layer of either doped or undoped silicon oxide. If the etch stop layer is doped silicon oxide, then the dielectric layers above and below the etch stop layer are undoped silicon oxide. If the etch stop layer is undoped silicon oxide, then the dielectric layers above and below the etch stop layer are doped silicon oxide. An etch chemistry containing  $C_2H_2F_4$  (and optionally  $CHF_3$ ) provides sufficient etch selectivity between undoped silicon oxide and various doped oxides for the undoped silicon oxide to act as an etch stop layer (or vice versa). The use of undoped silicon oxide can lead to a significant reduction in the total dielectric constant of dual damascene structures relative to otherwise identical dual damascene structures including a silicon nitride layer.

### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a dual damascene interconnect structure including an etch stop layer of undoped silicon oxide.

Fig. 2 shows a dual damascene interconnect structure, including an etch stop layer of undoped silicon oxide, formed on a substrate with a gate.

Figs. 3A-3D show a method of forming a dual damascene interconnect structure that includes an etch stop layer of undoped silicon oxide.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

A dual damascene interconnect structure according to the invention includes a contact dielectric layer, an etch stop layer of undoped silicon oxide on the contact dielectric layer, a trench layer on the etch stop layer, and a continuous electrically conductive interconnect passing through holes in the contact dielectric layer, the etch stop layer and the trench layer. The term "undoped" as used herein refers to a dopant concentration of less than 1.0 wt.%. Conversely, the term "doped" as used herein refers to a dopant concentration of greater than or equal to 1.0 wt.%.

Fig. 1 shows an embodiment of the interconnect structure according to the invention. In this embodiment contact dielectric layer 1 includes a hole passing through contact layer 1. Etch stop layer 2 is in direct contact with contact dielectric layer 1 and includes a hole passing through etch stop layer 2. The hole in etch stop layer 2 overlaps and aligns with the hole in contact dielectric layer 1, forming a hole passing through etch stop layer 2 and contact dielectric layer 1. Trench layer 3 is in direct contact with etch stop layer 2 and includes a trench passing through trench layer 3. The trench in trench dielectric layer 3 is wider than and overlaps the hole passing through etch stop layer 2 and contact dielectric layer 1. In other embodiments, the trench in trench dielectric layer 3 can be the same width as or smaller than the hole passing through etch stop layer 2 and contact dielectric layer 1. Continuous electrically conductive interconnect 4 is inside, and preferably fills, the trench in trench dielectric layer 3 and the hole passing through etch stop layer 2 and contact dielectric layer 1.

Contact dielectric layer 1 and trench dielectric layer 3 can each include a single dielectric material or multiple layers of the same or different dielectric materials. The dielectric material in the contact dielectric layer and the trench dielectric layer can be doped or undoped, provided that the dielectric material can be etched, in particular, chemically etched. Preferably, the dielectric material is a doped oxide including silicon. The doping can be provided by any conventional dielectric material dopant, including, for example, B, Al, Ga, In, C, Si, Ge, Sn, N, P, As, Sb, and F. The doped oxide can be doped  $\text{SiO}_x$ , where  $0 < x \leq 2$ , preferably  $1 < x \leq 2$ , more preferably  $1.5 \leq x \leq 2$ . Preferably, the doped oxide is a doped silicate glass, such as, for example, fluorosilicate glass (FSG), borosilicate glass (BSG), phosphosilicate glass (PSG) and/or borophosphosilicate glass (BPSG). The thickness of each

of the contact dielectric layer and the trench dielectric layer is not particularly limited. Preferably, the thickness of the contact dielectric layer is within the range of about 0.1 to 3.0  $\mu\text{m}$ , more preferably 0.2 to 2.0  $\mu\text{m}$ , even more preferably 0.3 to 1.0  $\mu\text{m}$ . Preferably the thickness of the trench dielectric layer is within the range of about 0.1 to 3.0  $\mu\text{m}$ , more preferably 0.15 to 1.5  $\mu\text{m}$ , even more preferably 0.2 to 1.0  $\mu\text{m}$ . For 0.18  $\mu\text{m}$  gate width technology, a typical value for the contact dielectric layer thickness may be about 0.6  $\mu\text{m}$ , and a typical value for the trench dielectric layer thickness may be about 0.3  $\mu\text{m}$ .

Etch stop layer 2 may contain undoped silicon oxide, such as undoped  $\text{SiO}_x$ , where  $0 < x \leq 2$ , preferably  $1 < x \leq 2$ , more preferably  $1.5 \leq x \leq 2$ . Etch stop layer 2 has a substantially lower rate of etching in a chemistry containing  $\text{C}_2\text{H}_2\text{F}_4$  (and optionally  $\text{CHF}_3$ ) than trench dielectric layer 3 and contact dielectric layer 1.

$\text{C}_2\text{H}_2\text{F}_4$  etch chemistry, for etching trench and contact dielectric layers, may further include one or more etchants of the formula  $\text{C}_x\text{H}_y\text{F}_z$ , where  $x = 1-6$ , preferably 1-4;  $y = 0-2x$ , preferably 0-x, more preferably 1 or 2; and  $z = (2x-2-y)$ ,  $(2x-y)$  or  $(2x+2-y)$ ; preferably a first etchant of the formula  $\text{C}_a\text{H}_b\text{F}_c$ , where  $a = 1$  or 2, preferably 1;  $b = 0-2$ , preferably 1 or 2, more preferably 1; and  $c = (2a+2-b)$ ; and/or a second etchant of the formula  $\text{c-C}_p\text{H}_q\text{F}_r$ , where "c-" means a cyclic ring of carbon atoms, preferably a cyclic ring of 3 or 4 carbon atoms;  $p = 3-6$ , preferably 3 or 4;  $q = 0-4$ , preferably 0-2, more preferably 0; and  $r = (2p-2-q)$  or  $(2p-q)$ , preferably  $(2p-q)$ . In specific embodiments, the first etchant may be selected from the group consisting of  $\text{CHF}_3$ ,  $\text{CF}_4$ ,  $\text{C}_2\text{F}_6$ , and combinations thereof, and is preferably  $\text{CHF}_3$ ; and the second (optional) etchant may be  $\text{c-C}_4\text{F}_8$ .

In an embodiment, for example, a flow rate for  $\text{C}_2\text{H}_2\text{F}_4$  may be approximately 2 sccm to 100 sccm, and preferably may be approximately 4 sccm to 40 sccm, and more preferably 6 sccm to 20 sccm. A flow rate for  $\text{CHF}_3$  may be approximately 0 sccm to 200 sccm, and preferably may be approximately 10 sccm to 150 sccm, and more preferably 30 sccm to 100 sccm. A flow rate for  $\text{C}_4\text{F}_8$  may be approximately 0 sccm to 100 sccm, and preferably may be approximately 2 sccm to 40 sccm, and more preferably 4 sccm to 20 sccm. A flow rate for Ar may be approximately 10 sccm to 300 sccm, and preferably may be approximately 20 sccm to 250 sccm, and more preferably 30 sccm to 200 sccm. A process pressure for such selective etch process may be approximately 10 mTorr to 200 mTorr, and preferably may be

approximately 20 mTorr to 150 mTorr, and more preferably 30 mTorr to 100 mTorr. A magnetic field supplied to the process chamber during the etch process may be approximately 0 G to 100 G, and preferably may be approximately 10 G to 70 G, and more preferably 20 G to 40 G. An RF power for the process may be approximately 200 W to 2000 W, and preferably may be approximately 300 W to 1500 W, and more preferably 400 W to 1000 W. A He cooling pressure for the wafer temperature control may be approximately 2 Torr to 60 Torr, and preferably may be approximately 4 Torr to 40 Torr, and more preferably 6 Torr to 20 Torr.

In accordance with the present invention, during the etching process using the  $C_2H_2F_4$  chemistry the etch rate ratio of the etch stop layer material to either the contact dielectric layer material or the trench dielectric layer material is independently  $\leq 1/8$ , preferably  $\leq 1/12$ , more preferably  $\leq 1/15$ . The etch stop layer typically will have a thickness of from about 100 to about 1,000 Å, preferably from about 200 to about 800 Å, more preferably from about 300 to about 700 Å.

Interconnect 4 can be any electrically conductive material. Preferably the interconnect is a metal or a metal alloy. Suitable metals include Al, Cu, W and Ti. Suitable metal alloys include Al-Cu, Al-Si-Cu, Al-Ge and Al-Si-Ge.

Fig. 2 shows an embodiment in which the interconnect structure of the present invention is formed on a gated substrate structure including an electrically conductive gate 6 on a substrate 5. The substrate 5 can include (not shown) electrically active semiconductor devices (each including, e.g., a source, a gated channel and a drain), metal lines and various dielectric regions. Although any semiconductor can be used, the active devices are preferably based on silicon. Gate 6 can have dielectric cap 7, and dielectric spacer 8, which separate gate 6 from contact dielectric layer 1 and electrically insulate gate 6 from conductive interconnect 4. Suitable caps and spacers may be formed by conventional methods known to those of ordinary skill in the art. For example, spacers can be formed by depositing a dielectric spacer material by LPCVD or PECVD, followed by anisotropically etching the deposited dielectric spacer material to form the spacer. A suitable dielectric spacer material may be selected by those of ordinary skill in the art and may provide a lower rate of etching relative to the surrounding contact dielectric material, thus protecting the gate 6 during



processing. For example, one suitable spacer material comprises a nitride such as silicon nitride (e.g. when the contact dielectric comprises an oxide). Typically, cap 7 will be about 100 Å to about 3,500 Å thick, preferably about 500 Å to about 2000 Å thick. Typically, spacer 8 will have a width, measured at the base, of from about 100 to about 1,500 Å, generally about 500 Å to 800 Å.

Between the interconnect 4 and the gated substrate an optional adhesion layer (not shown) can be used to promote the adhesion of interconnect 4 to the gated substrate. Suitable materials for adhesion layers are known in the art, and include, for example, Ti, Zr, Hf, Ta, Cr, Mo, W, Cu, Ni, Co, Ru, Rh, Pd, Os, Ir, Pt, Au, Ag, and alloys and (conductive) nitrides thereof. Interconnect 4 is preferably connected to an active device region in the substrate, either directly or through metal lines in the substrate 5.

The use of undoped silicon oxide (e.g., as an etch stop layer) can lead to a reduction in total dielectric constant in dual damascene structures. In conventional dual damascene structures, a silicon nitride etch stop layer is sandwiched between layers of silicon oxide. The silicon nitride increases the effective dielectric constant of the dual damascene structures. Replacing the silicon nitride with undoped silicon oxide eliminates a source of increased dielectric constant in dual damascene structures and can lead to a 10-40% reduction in total dielectric constant relative to an otherwise identical dual damascene structure having a silicon nitride etch stop layer.

Figs. 3A-3D illustrate a process for making a dual damascene interconnect structure according to the invention with an etch stop layer of undoped silicon oxide, which resists etching by the  $C_2H_2F_4$  chemistry. According to this embodiment, a gated substrate with a electrically conductive gate 6 on a substrate 5 is first provided by using conventional methods known to those of ordinary skill in the art. The gate 6 is covered with cap 7 and spacer 8 of one or more dielectric materials chosen so that the gate 6 is protected during subsequent processing.

Contact dielectric layer 1 is deposited on the gated substrate and planarized using a conventional film deposition and planarization techniques. Film deposition techniques, such as chemical vapor deposition or plasma-assisted vapor deposition, and planarization techniques, such as chemical-mechanical polishing, isotropic etching, and reflow techniques,

are known in the art.

Etch stop layer 2 is then deposited on contact dielectric layer 2, and resist layer 9 is deposited on etch stop layer 2. Resist layer 9 is exposed and developed to form a hole in resist layer 9 exposing the underlying etch stop layer 2. Lithographic patterning techniques using resists are well known in the art. Typically photoresists, both positive and negative, are used. As shown in Fig. 3A, the exposed portion of etch stop layer 2 is then etched using reactive ion etching and a conventional oxide etching gas chemistry, which is well known in the art, to form a via hole through etch stop layer 2 and into the underlying contact dielectric layer 1. Such chemistries may include reactive ion etching with an etchant of the formula  $C_xF_y$  (where  $x = 1-6$ , preferably 1-4, more preferably 1-2, and  $y = (2x-2)$ ,  $2x$  or  $(2x+2)$ , but is at least 4),  $C_aH_bF_c$  (as defined above),  $SF_6$ ,  $NF_3$ ,  $Cl_2$ ,  $HF$ ,  $HCl$ , and/or  $CCl_4$ . In one embodiment, the etch stop layer is etched using a chemistry comprising  $CHF_3$ ,  $CF_4$ , and/or  $C_2F_6$ , preferably a mixture of  $CHF_3$  and either  $CF_4$  or  $C_2F_6$ , optionally in the presence of Ar. Resist layer 9 is removed from etch stop layer 9 using conventional means known in the art.

Trench dielectric layer 3 is then deposited on etch stop layer 2 and planarized using conventional film deposition and planarization techniques. As shown in Fig. 3B, resist layer 10 is then deposited on trench dielectric layer 3 and patterned using conventional lithographic techniques to uncover portions of trench dielectric layer 3. As shown in Fig. 3C, the exposed portions of trench dielectric layer 3 are then etched by reactive ion etching using the above-described  $C_2H_2F_4$  (and optional  $CHF_3$ ) chemistry. Because the undoped silicon oxide of etch stop layer 2 resists etching by the  $C_2H_2F_4$  chemistry, only the trench dielectric layer material in, and the contract dielectric layer material below, the via hole in etch stop layer 2 is etched, preferably sufficiently to expose the substrate.

As shown in Fig. 3D, interconnect 4 is then formed by depositing a metal into the holes in the trench dielectric layer 3, etch stop layer 2 and contact dielectric layer 1, preferably filling the holes. The deposited metal is then planarized using conventional planarization techniques.

The process shown in Figs. 3A-3D represents only one of many methods of making the interconnect structure according to the present invention. Other methods are adaptations of conventional dual damascene processes, within the skill in the art, in which conventional

silicon nitride etch stop layers and associated etch chemistry are replaced with the undoped silicon oxide etch stop layer and  $C_2H_2F_4$  etch chemistry of the present invention (see, e.g., USSN 09/593,968, filed June 15, 2000, the relevant portions of which are incorporated herein by reference). Depending upon the particular dual damascene process adapted, the contact dielectric layer material and/or the trench dielectric layer material can be doped or undoped. In embodiments, the trench dielectric layer can be etched by  $C_2H_2F_4$ , which stops at the undoped silicon oxide of the etch stop layer. In other embodiments, such as is shown in Figs. 3A-3D, the trench dielectric layer can be etched with a gas chemistry, such as a chemistry containing  $CF_4$  and/or  $C_2F_6$ , that also etches the undoped silicon oxide etch stop layer. In these embodiments, subsequent etching with  $C_2H_2F_4$  can transfer the hole in the etch stop layer through the contact dielectric layer to the substrate without widening the hole in the etch stop layer.

In embodiments of the present invention, the trench dielectric layer, the etch stop layer and the contact dielectric layer are etched using a chemical etching technique, preferably reactive ion etching. Determination of process parameters for reactive ion etching is within the skill in the art. Etching gases useful in reactive ion etching include halocarbons such as  $CHF_3$ ,  $C_4F_8$ ,  $C_2F_6$ , F-134 (1,1,1,2-tetrafluoroethane), F-134a,  $CF_4$ ,  $SF_6$ ,  $NF_3$ ,  $SF_6$ ,  $Cl_2$ , HF, HCl,  $CCl_4$ , and mixtures thereof. The total flow rate of etching gas, including argon and/or carrier gases, is typically 5 to 500 SCCM, more preferably 15 to 300 SCCM and even more preferably 25 to 250 SCCM. Of this flow, up to 450 SCCM, preferably from 4 to 200 SCCM, may comprise a carrier gas such as Ne, Kr, Xe, CO,  $CO_2$ ,  $SO_2$ , He,  $O_2$ ,  $N_2$  and mixtures thereof.

In embodiments of the invention, a dual damascene process may include a step in which only a portion of the trench dielectric layer 3, the etch stop layer 2 or the contact dielectric layer 1 is etched. Under the etch conditions selected, an etching rate may be determined, and etching under the selected set of conditions may be conducted for a time sufficient to substantially remove the trench dielectric layer 3, the etch stop layer 2 or the contact dielectric layer 1 to a predetermined depth. The determination of the conditions and time(s) that provide such an etch is within the level of skill of those of ordinary skill in the art, and will typically take into consideration the thickness and composition of the trench

dielectric layer 3, the etch stop layer 2 or the contact dielectric layer 1, along with the parameters of the plasma. For example, a suitable etchant gas for etching a phosphorous-doped silicon dioxide trench dielectric layer 3 may comprise a mixture of  $C_2H_2F_4$ ,  $CHF_3$ ,  $C_4F_8$  and  $CF_4$ , and etching for about one minute under conditions providing an etch rate of approximately 3,000 Å per minute will remove about half of a 6,000 Å thick trench dielectric layer. In a further example, etching a phosphosilicate glass (PSG) dielectric layer with an etchant comprising F-134,  $C_4F_8$ , and  $CHF_3$  (Ar optional) at a total pressure of 10-300 mTorr (preferably about 55 mTorr), a magnetic field of 10-50 gauss (preferably about 30 gauss), and at a power of 100-2,500 W (preferably from about 500 to about 1,500 W) for a length of time of about 3 minutes, may be sufficient to remove from 8,000 to 9,000 Å of the dielectric layer at a rate of about 3,000 Å/min.

Semiconductor processing conditions that can be used in dual damascene processes are disclosed in U.S. Application Serial Nos. 08/577,751; 08/683,407; 08/693,978; 08/935,705; 09/253,991; and 09/326,432, and in U.S. Patent Nos. 5,468,342 and 5,562,801, the relevant portions of which are incorporated by reference herein.

While the present invention has been described with respect to specific embodiments, it is not confined to the specific details set forth, but includes various changes and modifications that may suggest themselves to those skilled in the art, all falling within the scope of the invention as defined by the following claims.

WHAT IS CLAIMED IS:

1. An interconnect structure comprising  
a contact dielectric layer;  
an etch stop layer over the contact dielectric layer;  
a trench dielectric layer over the etch stop layer; and  
an electrically conductive interconnect in (i) a hole through the contact dielectric layer  
and the etch stop layer, and (ii) a trench in the trench dielectric layer, wherein  
the etch stop layer comprises one member selected from a group consisting of an  
undoped silicon oxide and a doped silicon oxide; and each of the contact dielectric layer and  
the trench dielectric layer independently comprises the other member of the group.
2. The interconnect structure according to Claim 1, wherein the etch stop layer  
comprises an undoped silicon oxide, the contact dielectric layer comprises a first doped  
silicon oxide and the trench dielectric layer independently comprises a second doped silicon  
oxide.
3. The interconnect structure according to Claim 2, wherein the first and second  
doped silicon oxides independently further comprise at least one of fluorine, boron and  
phosphorus.

4. The interconnect structure according to Claim 2, wherein the first and second doped silicon oxides are independently selected from the group consisting of a fluorosilicate glass; a borosilicate glass; a phosphosilicate glass; and a borophosphosilicate glass.

5. The interconnect structure according to Claim 1, wherein the trench in the trench dielectric layer is wider than the hole through the etch stop and contact dielectric layers.

6. The interconnect structure according to Claim 1, further comprising  
a substrate; and  
a gate structure on the substrate in contact with the contact dielectric layer.

7. The interconnect structure according to Claim 6, wherein the substrate comprises silicon.

8. The interconnect structure according to Claim 6, wherein the gate structure comprises a gate dielectric layer over the substrate, a gate over the gate dielectric layer, a cap dielectric layer over the gate, and spacers adjacent to the gate and the cap dielectric layer.

9. The interconnect structure according to Claim 1, wherein the electrically conductive interconnect comprises a member selected from the group consisting of Al and Cu.

10. The interconnect structure according to Claim 1, wherein a thickness of the etch stop layer is from 100 Å to 1000 Å.

11. A method comprising selectively etching a trench dielectric layer and a contact dielectric layer in a structure comprising the trench dielectric layer, the contact dielectric layer, and an etch stop layer therebetween comprising undoped silicon oxide and having a hole therein, the hole containing a trench dielectric layer material, with an etch gas including  $C_2H_2F_4$ .

12. A method of forming an interconnect structure, the method comprising  
depositing an etch stop layer, containing an undoped silicon oxide, on a contact dielectric layer containing a first oxide comprising silicon;  
forming a hole through the etch stop layer;  
depositing a trench dielectric layer, containing a second oxide comprising silicon, on the etch stop layer and in the hole through the etch stop layer;  
forming a trench in the trench dielectric layer and a hole through the contact dielectric layer by etching the first and second oxides; and  
depositing an electrically conductive interconnect in the trench, the hole through the etch stop layer and the hole through the contact dielectric layer.

13. The method according to Claim 12, wherein forming the trench comprises etching the second oxide with a chemistry containing  $C_2H_2F_4$ .

14. The method according to Claim 13, wherein forming the hole through the etch stop layer comprises etching with a chemistry containing at least one of  $C_xF_y$  (where  $x = 1-6$ , and  $y = (2x-2)$ ,  $2x$  or  $(2x+2)$ , but is at least 4) and  $C_aH_bF_c$  (where  $a = 1$  or  $2$ ,  $b = 0-2$ , and  $c = (2a+2-b)$ ).

15. A method of forming an interconnect structure, the method comprising  
forming a trench in a trench dielectric layer;  
forming a first hole through an etch stop layer below the trench dielectric layer, the etch stop layer containing an undoped silicon oxide;  
forming a second hole through a contact dielectric layer below the first hole in the etch stop layer, the second hole being aligned with the first hole; and  
depositing an electrically conductive interconnect in the first hole, the second hole, and the trench.

16. The method according to Claim 15, wherein forming the trench comprises etching the second oxide with a chemistry containing  $C_2H_2F_4$  and stopping at the etch stop layer; or

etching the second oxide for a predetermined etch time with a chemistry containing at least one of  $C_xF_y$  (where  $x = 1-6$ , and  $y = (2x-2)$ ,  $2x$  or  $(2x+2)$ , but is at least 4) and  $C_aH_bF_c$ , (where  $a = 1$  or  $2$ ,  $b = 0-2$ , and  $c = (2a+2-b)$ ).



17. The method according to Claim 16, wherein forming the trench comprises etching with a chemistry containing  $C_2H_2F_4$ .

### ABSTRACT OF THE DISCLOSURE

A dual damascene interconnect structure, produced using etch chemistry based on  $C_2H_2F_4$ , includes (i) an etch stop layer of either undoped silicon oxide or doped silicon oxide, and (ii) dielectric layers both above and below the etch stop layer of the other (i.e., when the etch stop layer comprises undoped silicon oxide, the dielectric layers above and below the etch stop layer independently comprise a doped silicon oxide; and when the etch stop layer comprises doped silicon oxide, the dielectric layers above and below the etch stop layer independently comprise an undoped silicon oxide).

3	4	3
2		2
1		1

A hand-drawn floor plan of a house. The plan is divided into several rooms, each labeled with a number. At the bottom right is a front porch labeled '5'. To its left is a large living room labeled '1'. Above the living room is a kitchen labeled '2'. To the left of the kitchen is a dining area labeled '3'. To the left of the dining area is a bedroom labeled '4'. At the bottom left is a bathroom labeled '6', with a closet labeled '7' above it. The front porch (5) is at the bottom right. The living room (1) is a large area on the right. The kitchen (2) is at the top right. The dining area (3) is at the top left. The bedroom (4) is in the middle left. The bathroom (6) is at the bottom left, with a closet (7) above it.

FIG. 2

0964028-000400

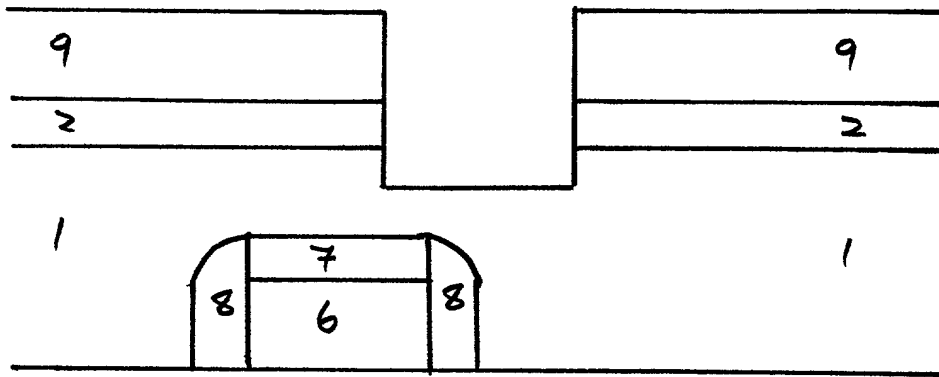


FIG. 3A

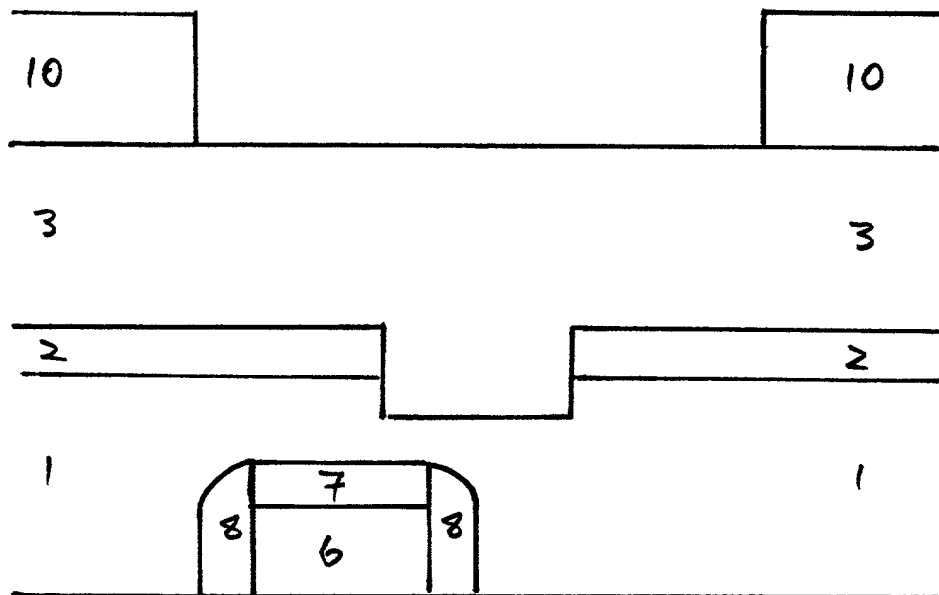


FIG. 3B



## Page 1 of 3

**My residence, post office address and citizenship are as stated below next to my name,**

# DUAL DAMASCENE STRUCTURE AND METHOD OF MAKING

☒ is attached hereto.

☐ was filed on \_\_\_\_\_ at \_\_\_\_\_

Application Serial No. \_\_\_\_\_

and amended on \_\_\_\_\_

☐ was filed as PCT international application

Number \_\_\_\_\_

On \_\_\_\_\_

and was amended under PCT Article 19

on \_\_\_\_\_ (if applicable).

We (I) acknowledge the duty to disclose information known to be material to the patentability of this application as defined in Section 1.56 of Title 37 Code of Federal Regulations.

We (I) hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed. Prior Foreign Application(s)

Application No.	Country	Day/Month/Year	Priority Claimed	
			<input type="checkbox"/> Yes	<input type="checkbox"/> No
			<input type="checkbox"/> Yes	<input type="checkbox"/> No
			<input type="checkbox"/> Yes	<input type="checkbox"/> No
			<input type="checkbox"/> Yes	<input type="checkbox"/> No

We (I) hereby claim the benefit under Title 35, United States Code, § 119(c) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

We (I) hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.


Application Serial No.	Filing Date	Status (pending, patented, abandoned)

And we (I) hereby appoint: Norman F. Oblon, Registration Number 24,618; Marvin J. Spivak, Registration Number 24,913; C. Irvin McClelland, Registration Number 21,124; Gregory J. Maier, Registration Number 25,599; Arthur I. Neustadt, Registration Number 24,854; Richard D. Kelly, Registration Number 27,757; James D. Hamilton, Registration Number 28,421; Eckhard H. Kuesters, Registration Number 28,870; Robert T. Pous, Registration Number 29,099; Charles L. Gholz, Registration Number 26,395; Vincent J. Sunderdick, Registration Number 29,004; William E. Beaumont, Registration Number 30,996; Steven B. Kelber, Registration Number 30,073; Robert F. Gnuse, Registration Number 27,295; Jean-Paul Lavalleye, Registration Number 31,451; Stephen G. Baxter, Registration Number 32,884; Martin M. Zoltick, Registration Number 35,745; Robert W. Hahl, Registration Number 33,893; Richard L. Treanor, Registration Number 36,379; Steven P. Weihrich, Registration Number 32,829; John T. Goolkasian, Registration Number 26,142; Marc R. Labgold, Registration Number 34,651; William J. Healey, Registration Number 36,160; Richard L. Chinn, Registration Number 34,305; Steven E. Lipman, Registration Number 30,011; Carl E. Schlier, Registration Number 34,426; James J. Kulbaski, Registration Number 34,648; Catherine B. Richardson, Registration Number 39,007; Richard A. Neifeld, Registration Number 35,299; and J. Derek Mason, Registration Number 35,270; our (my) attorneys, with full powers of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith; and we (I) hereby request that all correspondence regarding this application be sent to the firm of OBLON, SPIVAK, MCCLELLAND, MATER & NEUSTADT, P.C., whose Post Office Address is: Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202.

We (I) declare that all statements made herein of our (my) own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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8/31/00  
Date